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Electrical Measurement of SRAM Cell Variation and Sensitivity to Singe-Event Upsets by Low-Energy Protons

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Electrical Measurement of SRAM Cell Variation and Sensitivity to Singe-Event Upsets by Low-Energy Protons

Abstract

With the rise of the transistor in the 1970s, electronics shifted from analog circuitry, where values are stored on a continuum, to digital, in which ones and zeros are the law of the land. Transistors, as a class circuit element, can be affected by radiation and cosmic rays which then cause temporary or permanent failures, depending on the specifics of the situation. On Earth, this poses little risk with all electronics shielded by the magnetosphere, however for space bound electronics, the risks from these extraterrestrial particles are not so negligible. The first step in designing a mission to be able to survive upsets from energetic particles is to understand how these particles affect all the devices of a space-bound circuit. While this characterization historically assumes constant behavior across one chip, in this senior honors thesis I present an electrical characterization of cell level variations in upset probability by low-energy protons for a specific class of digital chip: SRAM. This characterization is possible because of random process variation in the manufacturing of the underlying transistors that is then responsible for variation in the critical charge to upset for each cell of an SRAM. The results of the electrical characterization are then related to upset data acquired by irradiating chips at the Vanderbilt University Pelletron. These data are used in conjunction with the cell level electrical characterization to discuss the effects of virtually screening out cells with higher probability to upset.

Keywords

SRAM, Radiation Effects, Single Event Upsets, Radiation Hardness Assurance

Cover Page Footnote

Science is the work of communities; not individuals. That is exceptionally true for this project which spanned two institutions and represents the culmination of my time as a Macalester student. As such, I have many folks I would like to thank. From the University of Tennessee at Chattanooga and the 2019 UTChattSat REU program, I would like to thank Daniel Loveless. Without his belief in me and support, absolutely none of this would have happened. Mandy McWeeney worked tirelessly behind the scenes to ensure that we had the materials we needed to do our work whether that was a circuit board that needed to be ordered or food when the dining hall was closed. Don Reising and Aldo McClean deserve thanks as well for their insightful comments over the course of the 10 weeks I was able to call Chattanooga my home-away-from-home. In my cohort, I want thank Giancarlo Vera as we both worked together to learn EAGLE and precision-soldering. I also want to thank Rafael Estrada for being my partner in developing the code to run the experiments. I want to thank Ryan Boggs for assisting me while preparing for his masters defense at the same time. For their work in preparation for the radiation experiments, I want to thank Gabriel Santos and Stephen Lawrence. Finally, Giancarlo and Kaitlin Hall deserve a special shout-out for being my rock-climbing buddies all summer; an activity we all enjoyed to de-stress after working all day in the labs. At Macalester, I need to thank Jim Doyle for being my advisor in all ways except officially for the physics major. He put up with me in no fewer than 5 courses as a student and thus is the single person most responsible for me succeeding academically. In preparation for extending this project from summer research to a full honors thesis, I found taking his topics course in Digital Electronics invaluable. I also need to thank my ``real" academic advisor Dr. Beth Cleary with whom I have been privileged to have taken three courses and acted in two productions she directed. She has been a rock of constant support for four years and I feel eternally grateful to her. Tom Finzell served as my on-campus advisor for this project and as such contributed immensely to the project through conversations and hours of whiteboard work. Tom, I enjoyed getting to know you and could not have completed this project with the quality of analysis it has without you. I want to thank Brianna Heggeseth and especially Ann Cannon for discussions of statistical analysis. I again want to thank Ann Cannon along with Scott and Chris Cannon for being my

family. They each contributed directly and indirectly to this project by giving me space to work over winter break and engaging in conversation about what I was doing. I love you all and your constant support means the world to me. Two of my friends and peers deserve my thanks for direct contributions to this project. Alyssa Bulatek assisted with the sensitivity analysis found in 2.2.1. Garrett Herring helped me optimize the experimental code while I was home for winter break. Orgho Neogi helped debug code and provided me with static proof foam. For being my friends and putting up with me during my four years at Macalester, I want to thank Maddie Outlaw, Alyssa Bulatek, Lilly Bralts-Kelly, Greta Helmel, James Crayton, Maya Wills, Ira Langdon, Luke Brown, Brooke Schneider, Missy Stevanovic, Elizabeth Fugikawa, Luke Bower, Brooke Schmolke, Sarah Coppenbarger, the inhabitants of Plearth, and all former, current, and future members of High Power Rocketry at Macalester. Finally, at Macalester I want to thank the stellar instructors and role models I have had the pleasure of interacting with: Tonnis ter Veldhuis, Andrew Beveridge, John Cannon, Sean Bartz, James Heyman, William Mitchel, Kristin Heysse, Anna Willams, Tom Finzell, Tom Barrett, Cheryl Moore Brinkley, Brian Adams, and Ken Moffett. While I am sure there are a million other folks I should also thank, this list must stop somewhere. If you do not find your name on this list but interacted with me at all during my four years at Macalester or during the last year as I worked on this project, know that I am deeply grateful for you.

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MACALESTER COLLEGE

Electrical Measurement of SRAM Cell Variation and Sensitivity to Single-Event Upsets by Low-Energy Protons

by

James Cannon

in the

Department of Physics and Astronomy

Advisor: T. Daniel Loveless

Macalester Project Advisor: Thomas Finzell

May 2020

"This thesis is dedicated to the lost class of 2020."

MACALESTER COLLEGE

Abstract

Department of Physics and Astronomy

by James Cannon

With the rise of the transistor in the 1970s, electronics shifted from analog circuitry, where values are stored on a continuum, to digital, in which ones and zeros are the law of the land. Transistors, as a class circuit element, can be affected by radiation and cosmic rays which then cause temporary or permanent failures, depending on the specifics of the situation. On Earth, this poses little risk with all electronics shielded by the magnetosphere, however for space bound electronics, the risks from these extraterrestrial particles are not so negligible. The first step in designing a mission to be able to survive upsets from energetic particles is to understand how these particles affect all the devices of a space-bound circuit. While this characterization historically assumes constant behavior across one chip, in this senior honors thesis I present an electrical characterization of cell level variations in upset probability by low-energy protons for a specific class of digital chip: SRAM. This characterization is possible because of random process variation in the manufacturing of the underlying transistors that is then responsible for variation in the critical charge to upset for each cell of an SRAM. The results of the electrical characterization are then related to upset data acquired by irradiating chips at the Vanderbilt University Pelletron. These data are used in conjunction with the cell level electrical characterization to discuss the effects of virtually screening out cells with higher probability to upset.

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CHAPTER 1: Introduction and Background

1.1 SRAM

Static Random Access Memory, or SRAM, devices are a particular class of digital device used for data storage. SRAM utilize dense arrays of memory cells to actively store data. Their cell density, power consumption, high read-write speeds, and cost makes SRAM attractive as a class of device used in space bound electronics for data storage (Seidleck et al. (1995), Austin et al. (2017), Sierawski et al. (2017), and Tonfat et al. (2016)). Fig. 1.1 schematically shows one SRAM cell. Data is stored via two logic inverters, otherwise known as NOT gates. The logic level, “high” or “low” corresponds to the supply voltage (V_{DD}) and ground (GND) respectively. A computer is then able to interpret “high” and “low” as a one and zero respectively. In Fig. 1.1, a logic low is applied to the first NOT gate. The NOT gate then draws from V_{DD} and outputs that logic high signal to the second NOT gate. With a logic high applied to the second NOT gate, it draws from its GND connection to output logic low back to the first NOT gate. This cycle of reinforcing logic levels through inverting complimentary signals makes SRAM a volatile class of digital memory: it requires active power in order for the data in a cell to continue being stored.

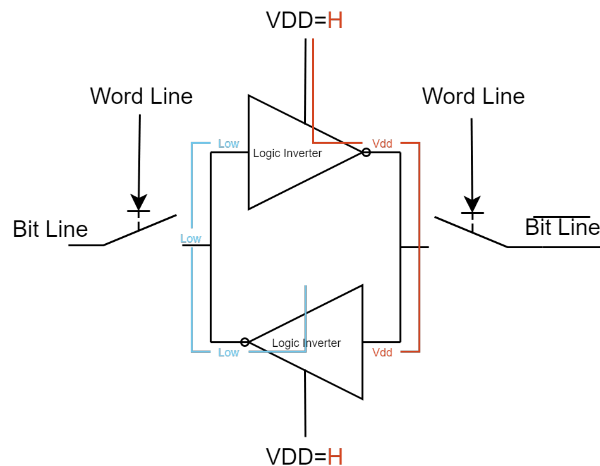

FIGURE 1.1: A schematic of a single SRAM cell.

The low cost makes commercial-off-the-shelf (COTS) SRAM especially attractive for these applications. However, the very same dense cell architecture that makes SRAM attractive, is part of what makes them highly susceptible to singe-event-upsets (SEUs).

1.2 Single Event Upsets

An SEU occurs in SRAM when an incident particle, like a proton, deposits enough charge to the cell to flip the value stored from a one to a zero or vice versa. The amount of charge necessary to cause an SEU is known as the critical charge, Q_c. Particularly unique to SRAM is the wide range of particle energy levels that can cause SEUs. SEU test results for unhardened SRAMs fabricated in highly scaled technologies indicate that the memory cells can be susceptible to upset by direct ionization by protons with linear energy transfer (LET) values less than 1 MeV-cm^2/mg (Heidel et al. (2008) and Pellish et al. (2014)).

1.2.1 Cross-Section

This susceptibility is measured quantitatively as a cross-section. A cross-section is determined by bombarding a chip with a range of particles with different LET values. Then, via Eqn. 1.1, a cross-section for each particle is calculated.

$$\sigma_{SEU} = \frac{\text{\# of upsets}}{\text{\# of particles/area}} \tag{1.1}$$

σ_{SEU} (cm^2) is the SEU cross-section (Schrimpf et al. (2008)). That it has units of area can lead to an interpretation of the cross-section being a measure of how much of a chip is sensitive to being hit by a particle. An analogous quantity is to normalize to a cross-section per bit as in Eqn. 1.2

$$\sigma_{SEU/\text{Bit}} = \frac{\#\text{ of upsets}}{(\#\text{ of particles/area}) * (\text{total }\#\text{ of bits})} \tag{1.2}$$

In this case, the area represented by $\sigma_{SEU/\text{Bit}}$ is the area of circuitry in an average SRAM cell that will cause the cell to upset if a particle is able to deposit Q_c or greater charge.

With data from particles at multiple LET values, a curve like Fig. 1.2 from Schrimpf et al. (2008) can be generated. A key characteristic of most SEU cross-section plots is a clear lower threshold, below which, no upsets are recorded and the cross-section is 0. Additionally, at high LET values, the cross-section will saturate and approach a constant. What this means is that up until some minimum LET value, particles are unable to deposit Q_c to a cell and no cells upset. When particles are able to deposit Q_c or greater charge to a cell, the likelihood a cell upsets is constant and depends on the area of circuitry that is sensitive to charge depositions.

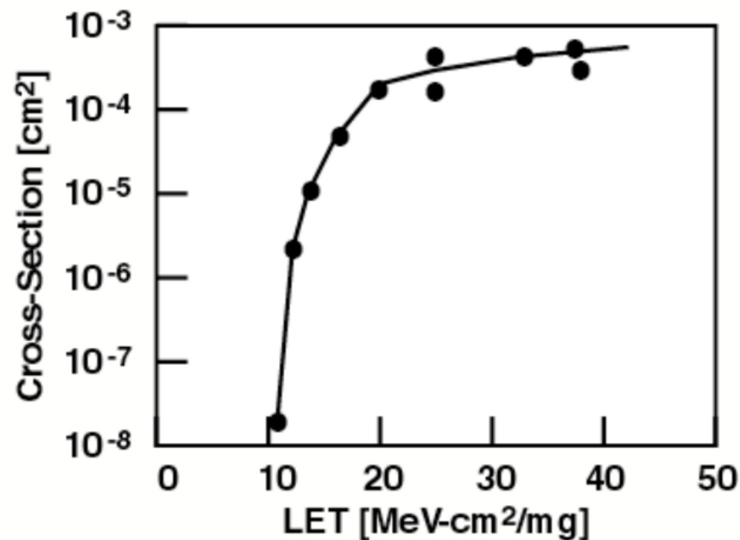

FIGURE 1.2: A typical SEU cross-section plot from Schrimpf et al. (2008) showing a clear threshold LET between 10-12 LET and a cross-section saturation of about $5 * 10^{-4}\text{cm}^2$

1.3 Critical Charge

Up until recently, it has been generally assumed that Q_c is a constant parameter for any given chip. That is, for a given chip every cell requires the same amount of charge in order to upset. Variability in SEU cross-section was then attributed to particles hitting a cell in different areas (Petersen (1996)). However, recent work by Loveless et al. (2010) and Heidel et al. (2009) show variability beyond that explainable by different hit areas. In particular, Loveless et al. (2010) in Fig. 1.3 show that while the different hit area argument is valid for LET values between 1 and 10 MeV-cm^2/mg, measured cross-sections for LET values below 1 MeV-cm^2/mg correspond to a nonphysically small area. This represents a subset of cells that have a lower Q_c value than the majority of the cells. Through physics-based simulations, they showed a maximum variability in Q_c of 22% for NMOS devices and 30% for PMOS devices.

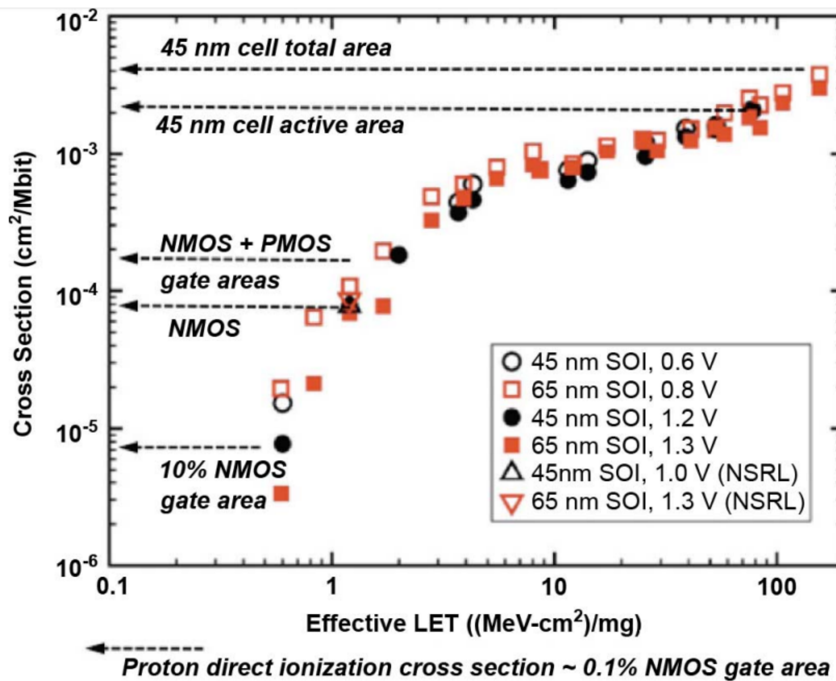

FIGURE 1.3: A cross-section LET curve from Loveless et al. (2010) with important areas shown on the y-axis. In particular, this plot shows the area represented by the cross-section produced from particles with LET under 1(MeV-cm^2)/mg are smaller than any physical susceptible area of a singe cell.

Kobayashi et al. (2020) (citing Kobayashi et al. (2018) and Wang et al. (2010)) discusses how Q_c can be effectively estimated via the data retention voltage, V_{DR}, with Eqn. 1.3.

$$Q_c = aC(V_{DD} - V_{DR}) \tag{1.3}$$

In Eqn. 1.3, a is a constant and C is the load capacitance (Kobayashi et al. (2020), Kobayashi et al. (2018), and Wang et al. (2010)). Importantly, Wang et al. (2010) show that a is a constant on the part-level and is immune to variations in either Q_c and V_{DR}. V_{DR} is the minimum voltage a cell needs to retain the data written to it. If data is written to a cell and V_{DD} is lowered below V_{DR}, that cell will have its upset. Thus, cells with lower than the average minimum holding voltages have larger Q_c than average. Likewise, the "weakest" cells, those with the highest minimum holding voltages, exhibit the lowest Q_c levels. This relationship is due to the inverse dependence of the cell's minimum holding voltage on the capacitive energy storage. Given V_{DR} for the cells of an SRAM, those cells can be assigned a Q_c accurate to within a constant, allowing the cells to be compared against each other and aggregate statistics to be pulled out.

Eqn. 1.3 allows Q_c to be predicted via a quantity that can be measured electrically. For this thesis, while measurements were only taken of the V_{DR} of cells, the data will generally be presented transformed to Q_c values relative to the chip's mean, $\overline{Q_c}$. A $Q_c = 1$ is exactly the mean of the chip.

CHAPTER 2: Experiment

The overall goal of this project is to characterize the Q_c individual cells within a commercially available SRAM chip and relate that to radiation cross-section data. If the chip can be characterized with an electrical test and the results of that characterization can be related to the chip's response when irradiated, that could have significant impacts in how space-bound electronics are qualified for use in missions. Given the two-fold goals—an electrical characterization of the Q_c value of every cell in a chip and the related characterization of every cell's response when irradiated—the methodology on collecting data is broken into those two parts.

2.1 Methodology

Several discrete chips where analyzed. Primarily, multiple chips of the 256 kByte MicroChip 23k256 were analyzed both in their Dual Inline Package (DIP) and Thin Shrink Small Outline Package (TSSOP) versions. Secondarily, the 256 kByte On Semiconducter N25S830HA in its TSSOP version was analyzed. To keep a unique identifier on each chip, the following 4 character key was employed: the prefix "A" or "B" corresponds to MicroChip devices or On Semiconducter devices respectively. The prefix "R" indicates a de-lidded MicroChip device that was irradiated after electrical characterization. The second letter being a "D" or a "T" indicates whether the device was a DIP or TSSOP packaged device respectively. The final two characters being numeric start a count from 01 to uniquely identify devices that are otherwise identical. Thus Device-Under-Test (DUT) AD03 indicates the third 256 kByte MicroChip 23K256 in a DIP package.

2.1.1 Electrical Characterization

Electrical characterization of each COTS SRAM was performed using the custom memory tester discussed in 2.2. Every logical byte was given the same value, or data pattern, to hold. One byte is comprised of eight logical bits. Every logic

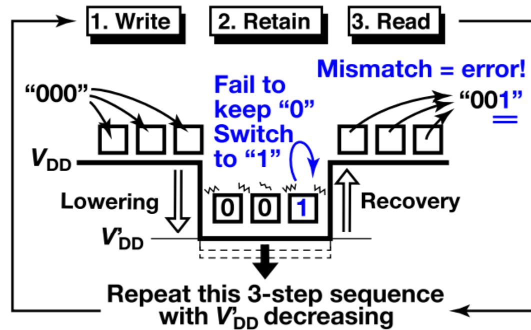

FIGURE 2.1: A graphical overview of the electrical characterization from Kobayashi et al. (2020)

'bit' is physically one discrete SRAM 'cell'. The value held by a bit is the same as the value held by a cell. Data patterns of 0x00 (all zeros), 0xFF (all ones), 0xAA (checkerboard, 10101010), and 0x55 (checkerboard, 01010101) were written to the memory, and the holding voltage (V_{HOLD}) reduced from the manufacturers recommended data retention voltage in increments of 2.44mV where it was held for two seconds. After the two-second hold time, the supply voltage was raised back to the nominal value, and each byte within the SRAM was read. Any discrepancies from the original data patterns were flagged, and the logical addresses of the failed

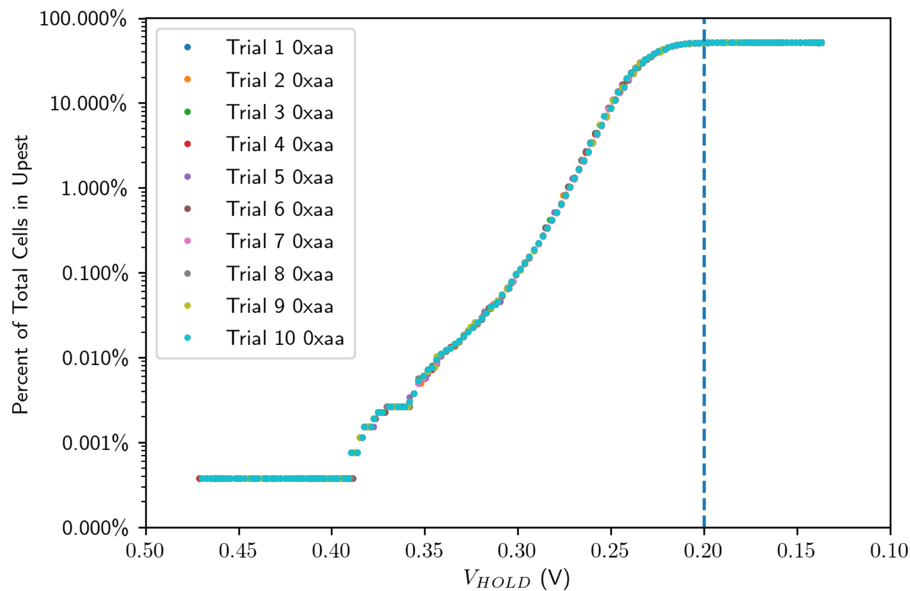

FIGURE 2.2: The percent of total cells reporting data retention failure versus the holding voltage (V_{HOLD}) for DUT AT01. The approximate saturation of cells in upset is noted by the blue dashed line at 0.2 V

cells recorded. Fig. 2.1 from Kobayashi et al. (2020) helps visualize the method used to electrically characterize a chip for a data pattern of 0x00.

This process was repeated until at least 50% of the SRAM cells reported failure, beyond which the failure pattern resembles the random distribution associated with the SRAM power cycle and represents the SRAM's power-up state described by Holcomb et al. (2009). Fig. 2.2 shows the percentage of total cells reporting data retention failure versus V_{HOLD} for AT01 across 10 trials. These data make it clear that the saturation of failed cells (greater than 50% of cells indicating failure) occurred at a V_{HOLD} of approximately 0.2V. Each DUT was characterized for holding voltages as low as 0.21V.

2.1.2 Radiation Characterization

Two de-lidded MicroChip 23k256 DIP chips (RD03 and RD04) were irradiated at the Vanderbilt University Pelletron with 1.8 MeV protons, corresponding to an LET of 0.12 MeVcm^2/mg. Before radiation exposure, each DUT was characterized using the methodology discussed in the previous section, for V_{HOLD} values between 0.607 V and 0.217 V. For each radiation trial, a beam flux of $4.00 * 10^6$ particles per second was used. The exposure time was varied from 5 seconds to 300 seconds to vary the fluence, or the total number of particles colliding with the chip.

During radiation exposure, the V_{HOLD} of the DUT was lowered to adjust the sensitivity to upset until SEUs were observed. Perhaps intuitively, if a chip is supplied with lower voltage than it is designed to operate with, it becomes more susceptible to upset. As expected, the DUT cross-sections increased with decreasing holding voltage, as seen in Fig. 2.3, where the SEU cross-sections versus holding voltage are plotted for parts RD03 (red circles) and RD04 (blue squares). Data were taken at a variety of exposure times and for holding voltages between 3.3v (nominal) and 0.45v, taking care to not lower V_{HOLD} below the highest recorded V_{DR} for each chip. After each test, the address of each upset bit was logged.

Despite RD03 and RD04 being identical components from the same manufacturer with the same package type, the different cross-section measurements highlights the heavy dependence on manufacture process variation of the cross-section at

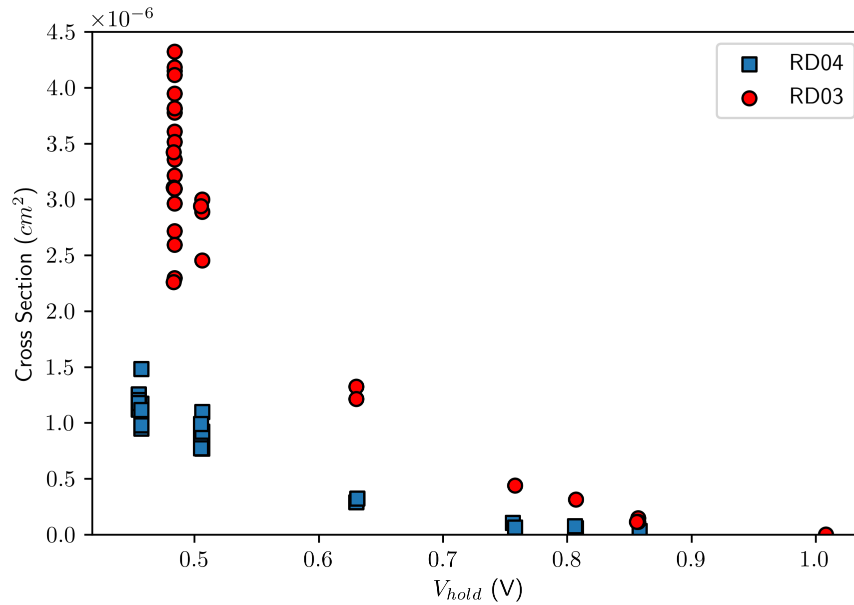

FIGURE 2.3: Measured SEU cross-sections (cm^2) for 2 MicroChip 23k256 SRAMs as a function of holding voltage (V) for 1.8 MeV protons.

these low LET levels. Fig. 2.4 shows the distribution of V_{DR} values of both RD03 and RD04 respectively. These distributions are normalized such that the sum of all bins totals one, representing a discrete probability density function. This shows that RD03 skews toward higher V_{DR} values for its cells than RD04 does, indicating lower Q_c values and thus larger cross-section measurements which is exactly what is seen in Fig. 2.3.

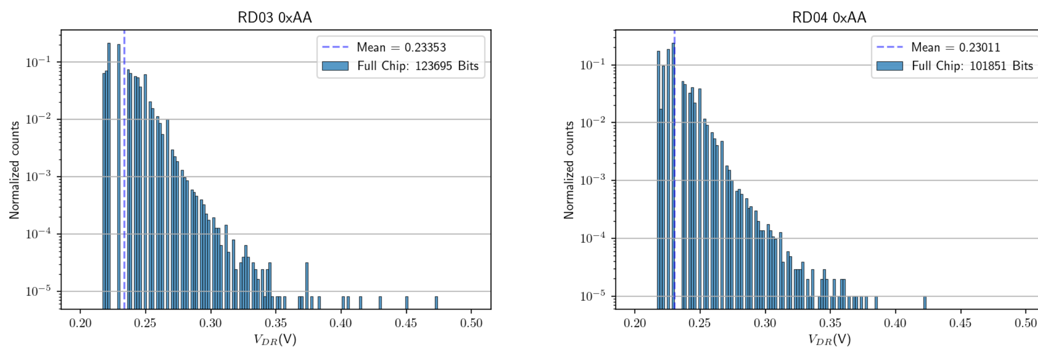

FIGURE 2.4: The distribution of V_{DR} values for characterized cells in RD03 and RD04 respectively. The mean value of each chip is noted by the dashed blue line. This shows RD04 to have generally higher V_{DR} values than RD03.

2.2 Experimental Design

To measure the V_{DR} of each cell of an SRAM chip, a custom circuit was designed and manufactured. Fig. 2.5 shows a conceptual diagram of the major elements of this circuit. The TI MSP430F2618 16-bit microcontroller unit (MCU) is the brains of the operation. It performs the logic required of the experiment and sends commands to all other devices in the circuit. The experiment was split into two discrete arrays, A and B, capable of simultaneously testing 12 and 8 SRAM chips respectively. The arrays are arranged spatially and the capacity of each array was determined by how many test zones could be placed on the Printed Circuit Board (PCB), shown in Fig. 2.6. The chips in each array received their power voltage, V_{dd} from independent voltage regulators. The regulators work by sending a constant $10\mu A$ current to the digital potentiometer. The voltage drop across the potentiometer is used to set voltage supplied to each memory array. So, the experiment runs by sending commands to the potentiometer to change its resistance, altering V_{dd} supplied to each array. Each digital potentiometer (AD5235 1024-position digital potentiometer from Anolog Devices) contains two

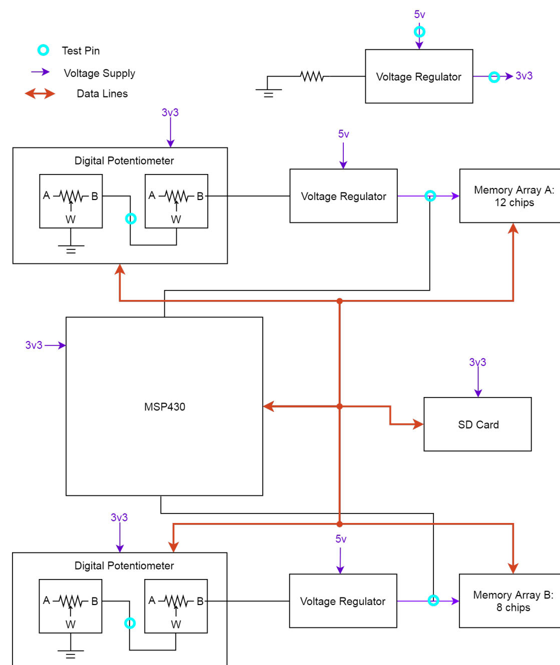

FIGURE 2.5: A high level circuit diagram showing the major components of the custom memory test developed for this project.

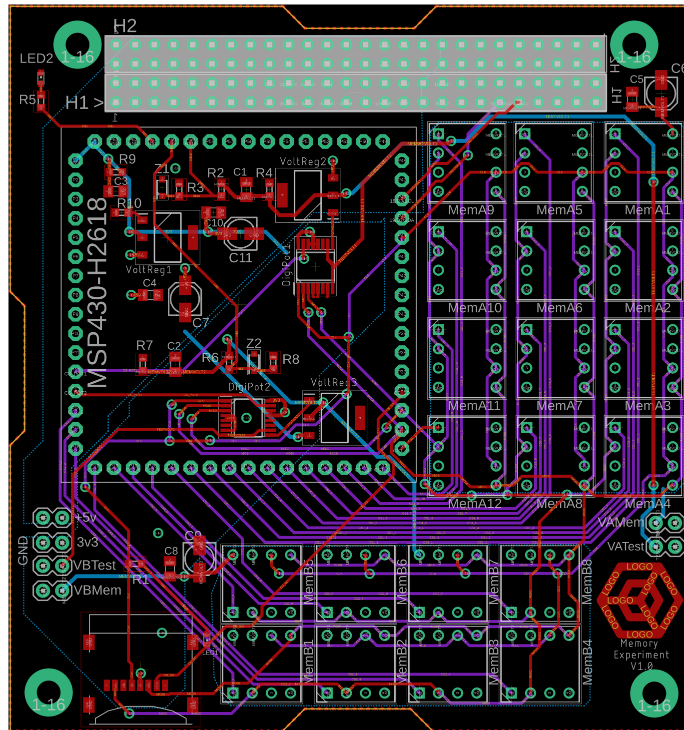

FIGURE 2.6: The PCB layout of the custom memory test circuit

$250k\Omega$ potentiometers which were wired in series to give each voltage regulator the ability send $10\mu A$ of current through variable resistance from $0 - 500k\Omega$ in 2048 discrete steps. This allows each memory array to receive programmable V_{dd} between $0 - 5V$ with a step size of $2.44mV$.

In practice, the actual circuit, whose board layout is shown in Fig. 2.6, has many more elements and is contained entirely on a 4-layer (PCB) that is smaller than 10cm x 10cm in area such that it could be flown in a 1U CubeSat. To decouple V_{dd} from any noise caused by clocked signals, all DC lines are routed on the bottom (blue) of the four layers. The next layer (orange) is exclusively a ground plane with clocked signals residing mostly in the third (purple) layer. The top (red) layer is used to make final connections to devices mounted exclusively on the surface of the PCB. Images of each distinct layer can be found in Appendix 2.2.

2.2.1 Sensitivity Analysis

To verify the voltage being sent to the memory arrays, each voltage regulator's output is also connected to an Analog-to-Digital-Converter (ADC) on the MCU and recorded. ADC's work by comparing the voltage at the terminal to discrete steps between GND and the MCU's V_{dd} which is $3.3V$. Given that the system is set-up to be able to sweep from $0 - 5V$, each line from a voltage regulator to an ADC passes through a voltage divider to scale $5V$ down to a maximum of $3.3V$. Each of these items—the MCU's Vdd, the bin size for the ADCs, and the resistance of the voltage dividers—all effect the sensitivity of the experiment and thus the reliability of saying an event occurred at a specific voltage. The relationship between the measured voltage, V_{ADC}, and the voltage at the DUTs, V_{Mem} is given by Eqn. 2.1.

$$V_{Mem} = V_{ADC} * \frac{R_A + R_B}{R_B} \tag{2.1}$$

where V_{Mem} is the voltage sent to the memory array, V_{ADC} is the value recorded by the ADC, and R_A and R_B make up the voltage divider. Factional uncertainties must be applied to determine the uncertainty in the voltage at the memory array. In Eqn. 2.2 $\delta(\ )$ indicates the uncertainty, or sensitivity, in the enclosed quantity.

$$\frac{\delta(V_{Mem})}{V_{Mem}} = \sqrt{\left(\frac{\delta(V_{ADC})}{V_{ADC}}\right)^2 + \left(\frac{\delta(\frac{R_A+R_B}{R_B})}{\frac{R_A+R_B}{R_B}}\right)^2} \tag{2.2}$$

Each ADC has 4096 bins and the reference voltage, which is nominally $3.3V$, was measured consistently to be $3.290V$ giving a $\delta(V_{ADC}) = \frac{3.290}{4096} = 8.032 * 10^{-4}V$. Taking a closer look at the second term, it is clear that the fractional uncertainty relationship must be applied to voltage divider equation. This gives Eqn. 2.3.

$$\frac{\delta(\frac{R_A+R_B}{R_B})}{\frac{R_A+R_B}{R_B}} = \sqrt{\left(\frac{\delta(R_A + R_B)}{R_A + R_B}\right)^2 + \left(\frac{\delta(R_B)}{R_B}\right)^2} \tag{2.3}$$

For the ADC attached to Memory Array A, $R_A = 3.390k\Omega$ and $R_B = 6.63k\Omega$ giving uncertainties of 0.5Ω and 5Ω respectively. Substituting these values into

Eqn. 2.3 gives $\frac{\delta(\frac{R_A+R_B}{R_B})}{\frac{R_A+R_B}{R_B}} = 9.328 * 10^{-4}$. Combining this result with the uncertainty in V_{ADC} and with Eqn. 2.2 and rearranging some terms gives Eqn. 2.4

$$\delta V_{Mem} = V_{Mem}\sqrt{\left(\frac{8.032 * 10^{-4}}{V_{ADC}}\right)^2 + \left(9.328 * 10^{-4}\right)^2} \tag{2.4}$$

Using Eqn. 2.1, this can be simplified to Eqn. 2.5 which is a function of V_{Mem}.

$$\delta V_{Mem} = \sqrt{8.7012 * 10^{-7}(V_{Mem})^2 + 1.9874 * 10^{-6}} \tag{2.5}$$

Following this process through for the values for the ADC attached to memory array B gives no variation in any significant digit. Fig. 2.7 shows the uncertainty graphed as a function of V_{dd}. The data reported in this thesis are entirely collected below $0.6V$ allowing the use of $1.53mV$ as an upper bound on the uncertainty on any given voltage measurement.

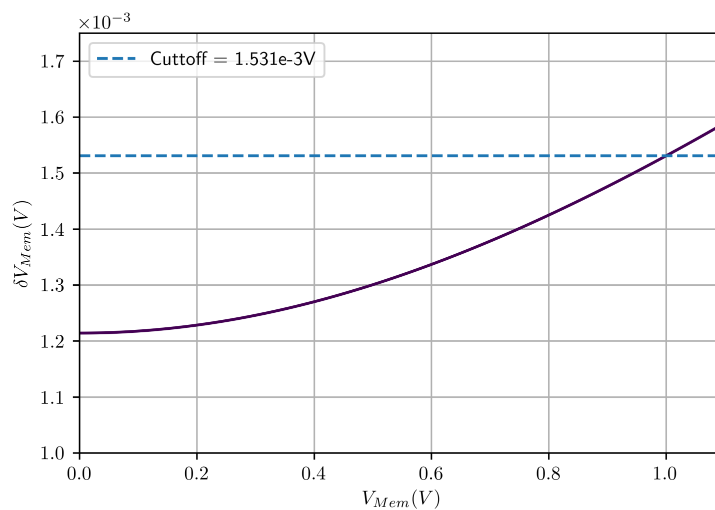

FIGURE 2.7: A plot of the uncertainty in the voltage measurements as a function of the voltage measured.

CHAPTER 3: Results

3.1 Electrical Data

The nominal supply voltage for the DUTs is 3.3 V, and the manufacturer's recommended minimum V_{HOLD} is 1.2 V. However, no parts reported failing cells for applied holding voltages of 0.5 V or greater. Fig. 3.1 illustrates an example spatial map of cell failures for a V_{HOLD} value of 0.277 V, where each white pixel represents one failed cell in DUT RD03. This "mapping" was made by taking each cell address, from 0 to 262143, and mapping it to a single pixel in a 512x512 image. While the actual physical relationship between cells is unknown, this and the following visualization show general behavior and are self-consistent in address-to-pixel mapping across trials. Also shown in the figure is a subset of cells for RD03 at various V_{HOLD} values, illustrating the onset for upset for multiple cells. These

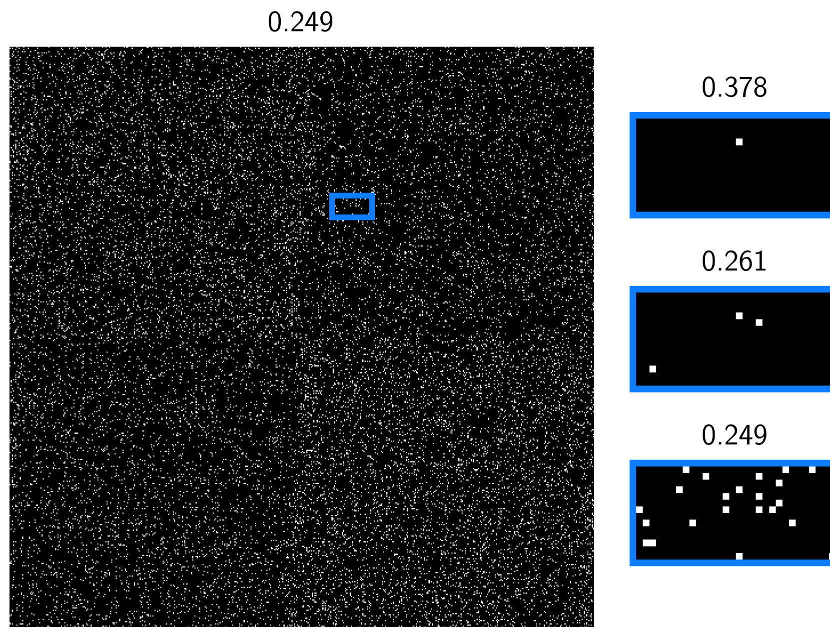

FIGURE 3.1: An example virtual spatial map of the failed cells for AD01 at $V_{HOLD} = 0.249$ V. Each white pixel represents one upset cell while black pixels indicate cells that retained stored data. A subset of cells for chip RD03 at V_{HOLD} values from 0.378 V to 0.249 V is also shown, illustrating that the same bits are seen to upset consistently once a threshold holding voltage is reached.

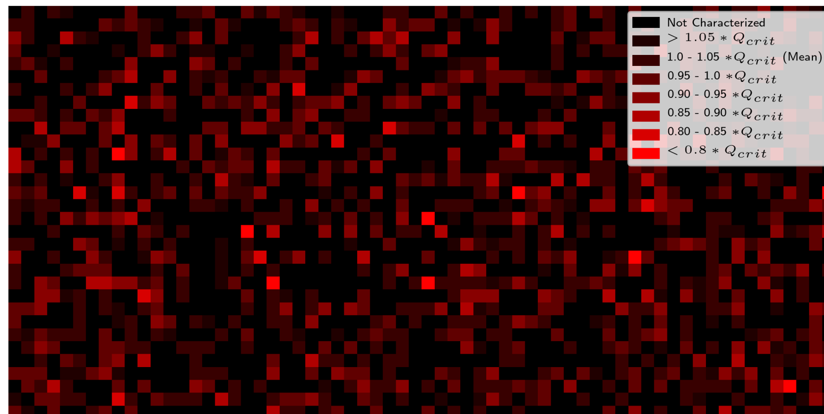

FIGURE 3.2: Example virtual spatial heat map of Q_c to upset for a subset of the cells in DUT RD03. Brighter red pixels have a lower relative Q_c, or are "weaker" than average. Black cells did not upset.

data show a high level of consistency with the same cell upsetting at subsequently lower V_{HOLD} values, even after having been re-initialized. This consistency is observed across multiple trials, indicating that every bit has some threshold V_{HOLD} below which it will upset. This provides confidence that each cell has a single and consistent V_{DR} value associated with it for particular data being held. Given V_{DR} for the cells of an SRAM, those cells can be assigned a Q_c accurate to within a constant via Eqn. 1.3 allowing the cells to be compared against each other and aggregate statistics to be pulled out. For the rest of this thesis, while measurements were only taken of the V_{DR} of cells, the data will be presented transformed to Q_c values relative to the chip's mean, $\overline{Q_c}$. A $Q_c = 1$ is exactly the mean of the chip.

An example of the spatial mapping of Q_c for the DUT RD03 is shown in Fig. 3.2. The bright red pixels represent cells with a lower Q_c. The black pixels represent cells that did not exhibit data retention failure.

Fig. 3.3 shows a histogram of Q_c for all cells within SRAM RD03. The distribution is normalized such that the mean Q_c has a value of one, and the sum of all bins totals one, representing a discrete probability density function. The chart illustrates that the range of Q_c is constrained primarily to $\pm 10\%$. However, several cells have extremely low critical charge values, showing up to a 25% decrease from the mean. This variability matches with calculations made by Loveless et al. (2010) with maximum variability of 22% and 30% for NMOS and PMOS strikes respectively.

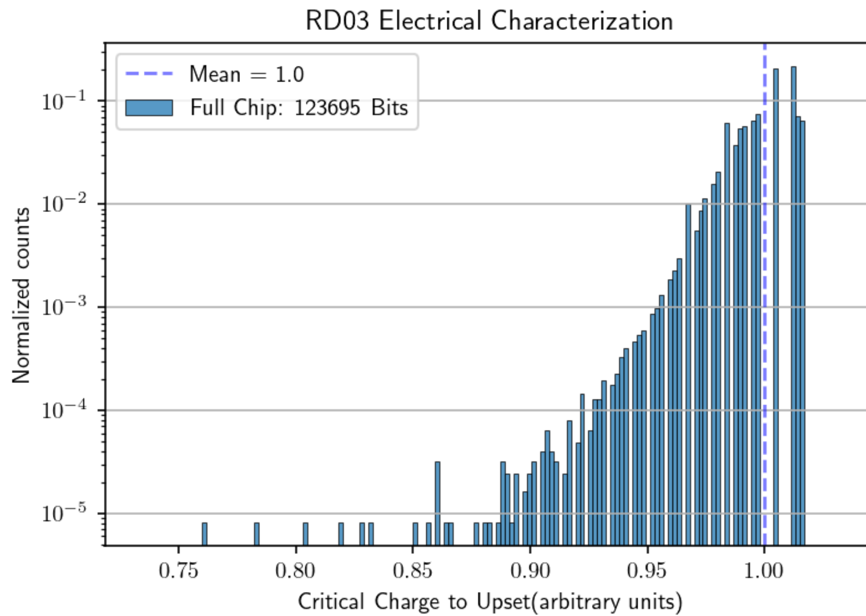

FIGURE 3.3: The distribution of Q_c for all cells electrically characterized in SRAM RD03. The mean is indicated as a dashed vertical line, and was normalized to a value of 1.

While other work (Kobayashi et al. (2018) and Kobayashi et al. (2020)) has shown these data to be Gaussian, these data match more closely with modeling predictions done by Wang et al. (2010). Wang et al. (2010)'s simulation predicted skewed data with a heavy tail toward higher V_{DR} values which corresponds to lower Q_c values. It is, however, a limitation of the testing procedure in which data were not taken for V_{Hold} lower than approx. 0.208V which likely accentuates the asymmetry of these data. Further compounding this, chips RD03 and RD04 were only characterized to 0.217V due to time constraints with the chips before irradiation. This 0.009V discrepancy is equivalent to four steps or bins in the histograms reported skewing data from these chips further.

These distributions form the foundation for the analysis post-radiation.

3.2 Radiation Data

For the radiation data, there were two chips, RD03 and RD04, which were irradiated 33 and 30 discrete times for which data were collected. Tbl. 3.1 and 3.2 show the conditions of each test as well as tracking the total ionizing dose (TID) of each DUT. From these aggregate data, Fig. 2.3 was created. However, of primary interest is exactly which bits flipped. Specifically, were the bits that were identified as having lower than average Q_c values more likely to flip than those with higher Q_c?

TABLE 3.1: RD03 Test Conditions

Trial #	Δt_{rad} (sec)	Fluence (# of particles)	Cumulative TID (rads)	V_{hold} (V)	# of Bits Flipped
B*				0.50511	0
1	30	$1.20 * 10^8$	$2.30 * 10^2$	0.50632	347
2	30	$1.20 * 10^8$	$4.61 * 10^2$	0.50632	360
3	90	$3.60 * 10^8$	$1.15 * 10^3$	0.50632	884
4	30	$1.20 * 10^8$	$1.38 * 10^3$	0.50511	353
5	5	$2.00 * 10^7$	$1.42 * 10^3$	0.48447	83
6	10	$4.00 * 10^7$	$1.50 * 10^3$	0.48447	173
7	15	$6.00 * 10^7$	$1.61 * 10^3$	0.48447	251
8	20	$8.00 * 10^7$	$1.77 * 10^3$	0.48447	305
9	25	$1.00 * 10^8$	$1.96 * 10^3$	0.48447	336
10	30	$1.20 * 10^8$	$2.19 * 10^3$	0.48447	433
11	45	$1.80 * 10^8$	$2.53 * 10^3$	0.48447	633
12	60	$2.40 * 10^8$	$3.00 * 10^3$	0.48447	772
13	75	$3.00 * 10^8$	$3.57 * 10^3$	0.48447	929
14	90	$3.60 * 10^8$	$4.26 * 10^3$	0.48447	1067
15	120	$4.80 * 10^8$	$5.18 * 10^3$	0.48447	1305
16	150	$6.00 * 10^8$	$6.34 * 10^3$	0.48447	1557
17	180	$7.20 * 10^8$	$7.72 * 10^3$	0.48447	1655

*Baselines were conducted in the chamber with a flux of zero to ensure no TID affects

Trial #	Δt_{rad} (sec)	Fluence (# of particles)	Cumulative TID (units)	V_{hold} (V)	# of Bits Flipped
18	210	$8.40 * 10^8$	$9.33 * 10^3$	0.48325	1901
B*		0	$9.33 * 10^3$	0.48447	0
19	30	$1.20 * 10^8$	$9.56 * 10^3$	0.48325	373
20	60	$2.40 * 10^8$	$1.00 * 10^4$	0.48447	744
21	45	$1.80 * 10^8$	$1.04 * 10^4$	0.48447	680
22	15	$6.00 * 10^7$	$1.05 * 10^4$	0.48447	237
23	15	$6.00 * 10^7$	$1.06 * 10^4$	0.48447	247
24	15	$6.00 * 10^7$	$1.07 * 10^4$	0.48447	229
25	30	$1.20 * 10^8$	$1.09 * 10^4$	0.48325	411
B*		0	$1.09 * 10^4$	0.48447	0
B*		0	$1.09 * 10^4$	0.85845	0
26	30	$1.20 * 10^8$	$1.12 * 10^4$	0.85723	18
27	30	$1.20 * 10^8$	$1.14 * 10^4$	0.63017	159
B*		0	$1.14 * 10^4$	0.80745	0
28	30	$1.20 * 10^8$	$1.16 * 10^4$	0.80745	38
29	30	$1.20 * 10^8$	$1.19 * 10^4$	0.75767	53
B*		0	$1.19 * 10^4$	0.85723	0
30	30	$1.20 * 10^8$	$1.21 * 10^4$	0.85723	14
31	30	$1.20 * 10^8$	$1.23 * 10^4$	0.85602	14
32	30	$1.20 * 10^8$	$1.26 * 10^4$	0.63017	146
33	300	$1.20 * 10^9$	$1.49 * 10^4$	1.00779	3
B*		0	$1.49 * 10^4$	0.70667	0

*Baselines were conducted in the chamber with a flux of zero to ensure no TID affects

Table 3.2: RD04 Test Conditions

Trial #	Δt_{rad} (sec)	Fluence (# of particles)	Cumulative TID (rads)	V_{hold} (V)	# of Bits Flipped
CAL†	—	—	$6.37 * 10^2$	—	—
1	90	$3.60 * 10^8$	$1.33 * 10^3$	3.31359	0
2	90	$3.60 * 10^8$	$2.02 * 10^3$	0.50632	278
3	60	$2.40 * 10^8$	$2.48 * 10^3$	0.50511	227
B*	—	0	$2.48 * 10^3$	0.50632	0
4	30	$1.20 * 10^8$	$2.71 * 10^3$	0.50632	107
5	30	$1.20 * 10^8$	$2.94 * 10^3$	0.50511	96
6	30	$1.20 * 10^8$	$3.17 * 10^3$	0.50511	105
7	30	$1.20 * 10^8$	$3.40 * 10^3$	0.50632	132
B*	—	0	$3.40 * 10^3$	0.50632	0
8	30	$1.20 * 10^8$	$3.63 * 10^3$	0.50511	97
9	30	$1.20 * 10^8$	$3.86 * 10^3$	0.50632	111
10	30	$1.20 * 10^8$	$4.09 * 10^3$	0.50511	119
11	30	$1.20 * 10^8$	$4.32 * 10^3$	0.50511	93
B*	—	0	$4.32 * 10^3$	0.76009	0
12	30	$1.20 * 10^8$	$4.55 * 10^3$	0.75645	13
13	30	$1.20 * 10^8$	$4.78 * 10^3$	0.75767	8
NA**	30	$1.20 * 10^8$	$5.01 * 10^3$	(0.75)	(12)
B*	—	0	$5.01 * 10^3$	0.80745	0
14	30	$1.20 * 10^8$	$5.25 * 10^3$	0.80623	4
15	30	$1.20 * 10^8$	$5.48 * 10^3$	0.80745	7
16	30	$1.20 * 10^8$	$5.71 * 10^3$	0.80745	4
17	120	$4.80 * 10^8$	$6.63 * 10^3$	0.80623	37
18	30	$1.20 * 10^8$	$6.86 * 10^3$	0.63017	35

*Baselines were conducted in the chamber with a flux of zero to ensure no TID affects

† Beam Calibration

** Test data not recorded. These trials have no bit addresses and voltage is assumed not measured.

Trial #	Δt_{rad} (sec)	Fluence (# of particles)	Cumulative TID (units)	V_{hold} (V)	# of Bits Flipped
19	30	$1.20 * 10^8$	$7.09 * 10^3$	0.63139	39
NA**	30	0	$7.32 * 10^8$	(0.625)	(43)
B*	—	0	$7.32 * 10^3$	0.63017	0
B*	—	0	$7.32 * 10^3$	0.45654	0
B*	—	0	$7.32 * 10^3$	0.45654	0
20	30	$1.20 * 10^8$	$7.55 * 10^3$	0.45654	141
21	30	$1.20 * 10^8$	$7.78 * 10^3$	0.45654	178
22	30	$1.20 * 10^8$	$8.01 * 10^3$	0.45533	151
23	180	$7.20 * 10^8$	$9.39 * 10^3$	0.45654	685
B*	—	0	$9.39 * 10^3$	0.45533	0
24	120	$4.80 * 10^8$	$1.03 * 10^4$	0.45654	509
25	30	$1.20 * 10^8$	$1.05 * 10^4$	0.45533	145
26	90	$3.60 * 10^8$	$1.12 * 10^4$	0.45533	403
27	60	$2.40 * 10^8$	$1.17 * 10^4$	0.45533	283
28	120	$4.80 * 10^8$	$1.26 * 10^4$	0.45654	537
B*	—	0	$1.26 * 10^4$	0.45654	0
29	180	$7.20 * 10^8$	$1.40 * 10^4$	0.45654	706
30	180	$7.20 * 10^8$	$1.54 * 10^4$	0.85845	25
B*	—	0	$1.54 * 10^4$	0.85723	0

*Baselines were conducted in the chamber with a flux of zero to ensure no TID affects

† Beam Calibration

** Test data not recorded. These trials have no bit addresses and voltage is assumed not measured.

To answer that question, histograms were plotted of the Q_c values of *only* the bits that flipped in a specific radiation test. These histograms were normalized the same way the electrical characterizations were in that the sum of all columns is equal to 1. For the sake of comparison, these distributions were plotted along with the baseline distribution. Fig. 3.4 shows an example of this with the 10th radiation trial. Bits that flipped but didn't have a corresponding electrical characterization

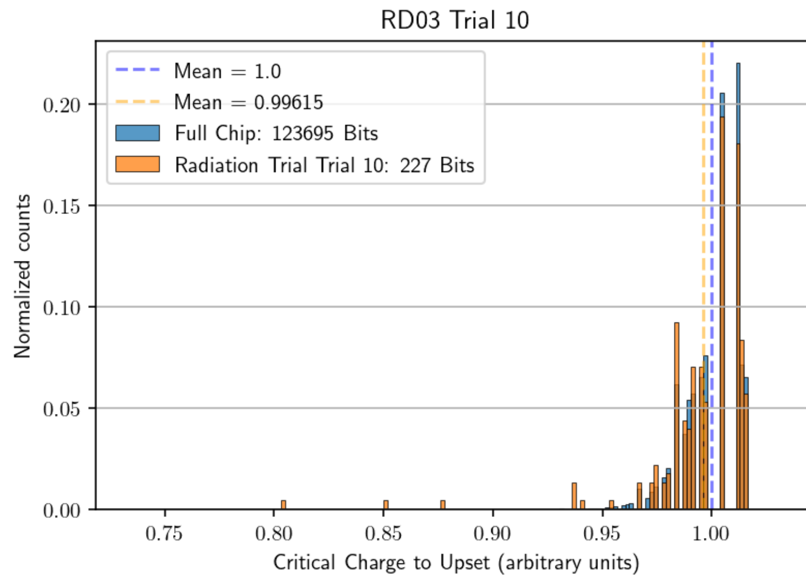

FIGURE 3.4: The distribution of relative Q_c values of the bits that flipped when RD03 was irradiated plotted on top of the full distribution of Q_c values for RD03. The mean value for each distribution is noted by a dashed line.

were discarded from the analysis which is why the legend lists 227 bits used in the distribution while Tbl. 3.1 lists 433 upsets from that same test. Just like with the plots of the electrical characterization, the mean of the data was calculated for the distribution. In Fig. 3.4, the mean Q_c values for cells reporting an SEU was approximately 0.4% lower than the chip average.

Fig. 3.5 shows two scatter plots the mean Q_c values from each of the sub-distributions created from the radiation trials for both chips (RD03 and RD04). The $\overline{Q_c}$, normalized to be 1, for each DUT is also shown as a solid line for visual clarity. There is a significant skew toward lower values of Q_c to upset in the cells that upset during these trials.

For DUT RD03, 29 out of 33 trials had mean (Q_c) values lower than the device mean. A Randomization Test for a Mean using 100,000 randomization samples on these data was conducted. The null hypothesis of a true mean equal to 1 was used for the test. For RD03, the p-value was reported to be 0.000070, giving extremely strong evidence to reject the null hypothesis. This indicates that there is statistically significant evidence that the mean Q_c for cells reporting SEU during proton irradiation is below the DUT mean Q_c. Said another way, the distribution

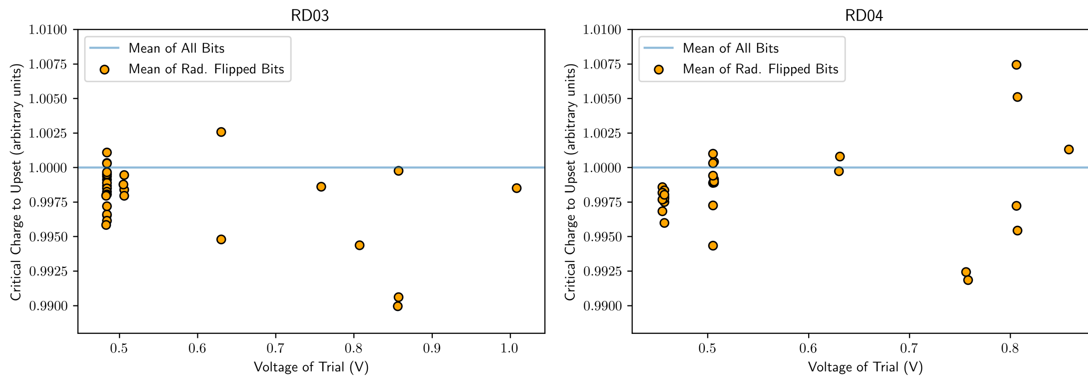

FIGURE 3.5: Scatterplots of the mean values of Q_c for cells reporting SEUs during all radiation trials for both MicroChip SRAM DUTs (left-RD03 and right-RD04). The average Q_c for each DUT is also shown as a solid line.

of bits upsetting when struck by low-energy protons in this device skews towards bits identifiable as "weak" via the electric characterization presented in 2.1.1.

DUT RD04 had 22 out of 29 trials with mean Q_c values below the device mean. Conducting the same statistical tests for the data as described above gives a P-value of 0.0067. While this is considerably greater than the P-value for DUT RD03, this is nonetheless approximately an order of magnitude better than the typical cut-off of 0.05 for a P-value to be reported 'statistically significant'. This indicates that it is extremely unlikely that these means would be reported in the case that the true mean of irradiated cells is equal to the mean of all cells electrically characterized. SEUs for both chips exhibited a statistically significant and consistent favoring of cells with lower Q_c than the mean of the chip, indicating that for a 1.8 MeV proton, nominally weak cells have a more than random chance of upsetting and thus can be screened out electrically.

3.3 Affecting the Cross-section

Having confirmed that there is significant evidence for weak bits to be more likely to upset when exposed to low energy radiation, we attempted to mitigate the upset cross-section through a 'virtual screen'. To do so, the data input to Eqn. 1.2 to calculate the $\sigma_{SEU/\mathrm{bit}}$ were modified. Screening thresholds were set at various Q_c values from $0.970 * \overline{Q_c}$ to $1.012 * \overline{Q_c}$. Cells with Q_c values lower than the screening

threshold were discounted as upset events. The total number of cells with Q_c values lower than the screening threshold was subtracted from the total number of bits used in Eqn. 1.2. This leads to Eqn. 3.1.

$$\sigma_{SEU/\text{Bit}} = \frac{(\#\text{ of upsets}) - (\#\text{ of upsets of cells below } Q_{c,thresh})}{(\#\text{ of particles/area}) * (\text{total } \#\text{ of bits} - \text{total } \#\text{ cells below } Q_{c,thresh})} \tag{3.1}$$

The first screen applied is to simply remove all bits for which there is no electrical characterization. Fig. 3.6 shows both the initial $\sigma_{SEU/\text{bit}}$ and the baseline screened $\sigma_{SEU/\text{bit}}$ for RD03 calculated for each of 32 trials. While applying this baseline screening gives a $\sigma_{SEU/\text{bit}}$ that is similar to the original, it is consistently higher. On average, the characterized cells have a $\sigma_{SEU/\text{bit}}$ 1.183 times that of all the cells. This mean, across these 32 trials, has a standard deviation of 0.163. While maybe not immediately obvious, it does make sense that the cross-section of only

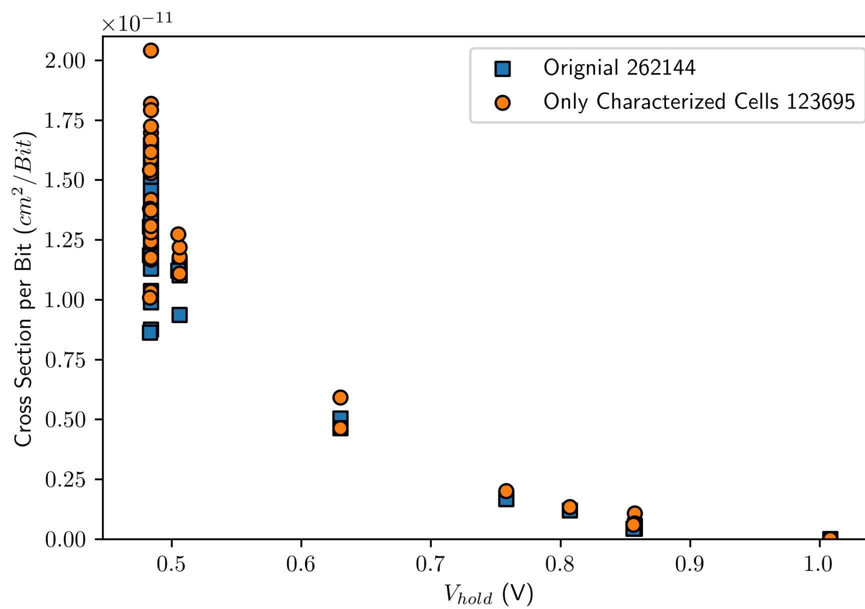

FIGURE 3.6: A plot of measured σ_{SEU}/bit. The blue squares are calculated from the raw data including all bit flips while the orange circles are calculated only using bits that had characterized Q_c values. These data plot all 32 trials for DUT RD03

the characterized cells is higher than that of the full chip and the reason for that comes from a limitation in how RD03 and RD04 were initially characterized.

As noted in 3.1, due to time constraints, RD03 and RD04 were only characterized down to 0.217V or approximately $1.02 * \overline{Q_c}$. As a result, the data are left skewed. This means that it is very likely the characterized cells as a group are "weaker" than the true average of the chip. So, when we consider only the characterized cells, the cross-section—which represents a probability of upset—increases. Then, to evaluate whether any further screening is effective at reducing the cross-section, the cross-section per bit of the *characterized* cells will be used as the baseline.

Virtual screens were applied at a variety of Q_c thresholds. To do this, when reading in the addresses of flipped bits, a flip was only counted if the cell it corresponded to had a Q_c value higher than the threshold value being used. Then the cross-section was calculated using Eqn. 1.2. The total number of bits used to normalize the data was the total number of cells with Q_c larger than the threshold. Fig. 3.7 shows these data for the baseline and two threshold values. It is difficult to say

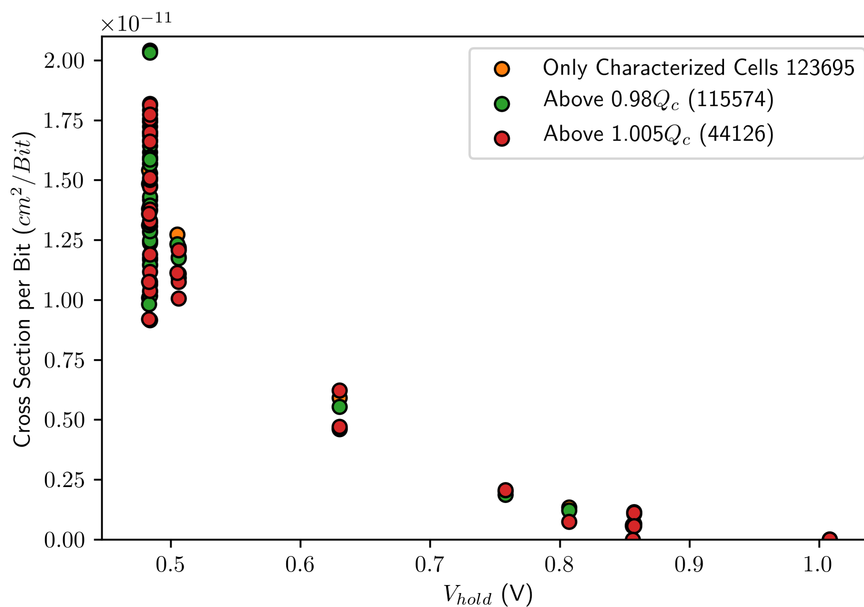

FIGURE 3.7: This plot of σ_{SEU}/bit for the baseline and two virtual screening thresholds is hard to draw conclusions from. It appears that the higher the screening threshold, the lower the σ_{SEU}/bit.

there's a trend although it *seems* that higher Q_c screening thresholds leads to a lower cross-section per bit.

To check, 15 threshold values were chosen for both RD03 and RD04. For each threshold, the ratio of the screened per bit cross-section divided by the baseline was calculated for each radiation trial. This converted into a percent change. A value of -10 for $0.98Q_c$ would indicate that for one of the 32 radiation trials for RD03, virtually screening out all cells with Q_c lower than $0.98*\overline{Q_c}$ lowered the σ_{SEU} by 10%. Fig. 3.8 shows two plots of how each of the 15 different threshold values affects the cross-section as a function of what percentage of bits were discarded for RD03 and RD04 respectively. Each screening case is represented as a box plot with the median value as a solid orange line. As is normal for box plots, the box represents the middle 50% data. Outliers are noted with green diamonds. This plot is zoomed in to show detail when a small fraction of bits are screened out. Fig. 3.9 shows the box plots for all data.

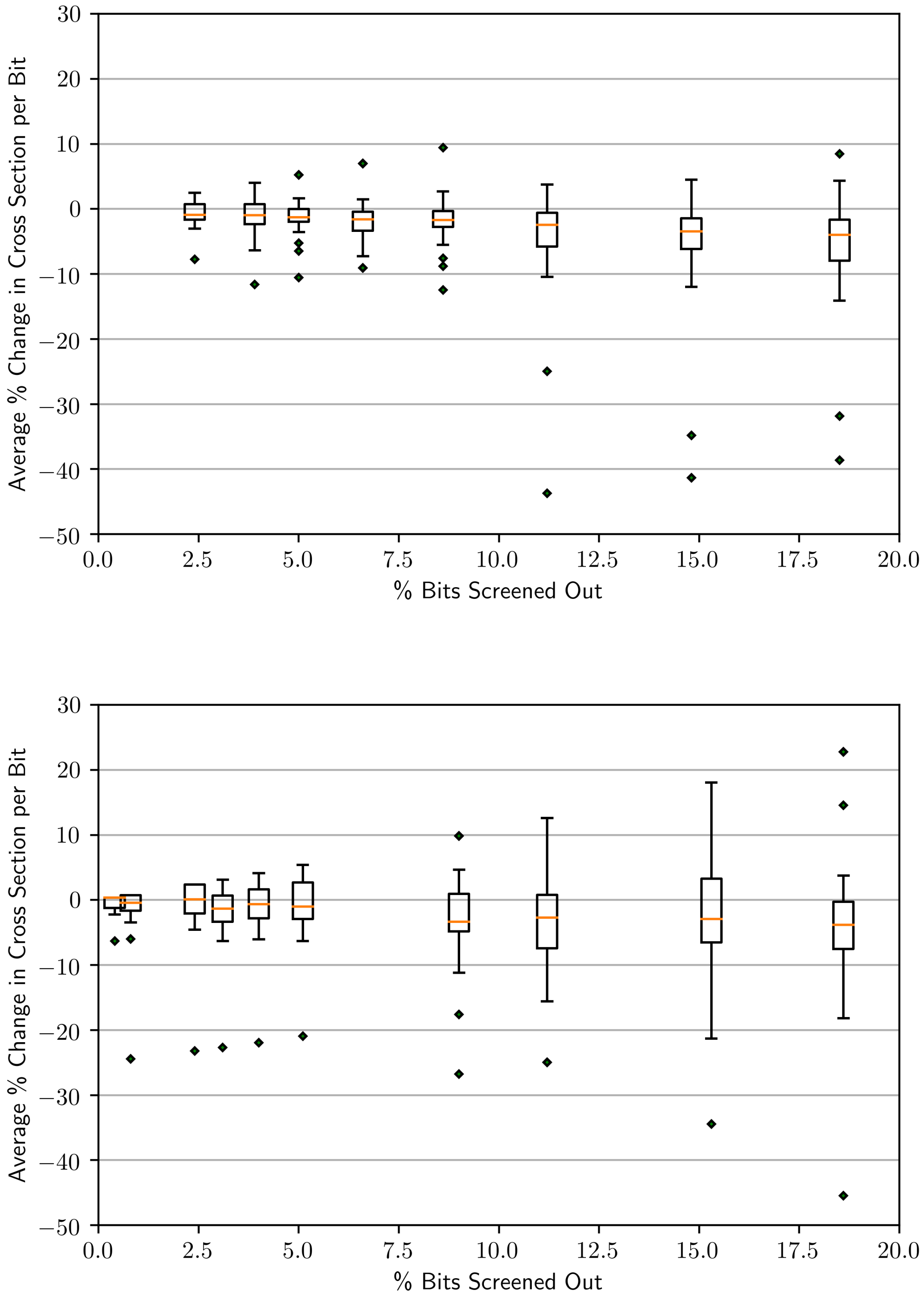

FIGURE 3.8: A plot of the average percentage change in σ_{SEU}/bit as a function of the percentage of bits screened out. RD03 results are shown on top and RD04 on bottom. In all cases, cells with Qc values above a certain threshold are kept and all others discarded. This plot is zoomed in to show detail in 0-20% of bits screened out range.

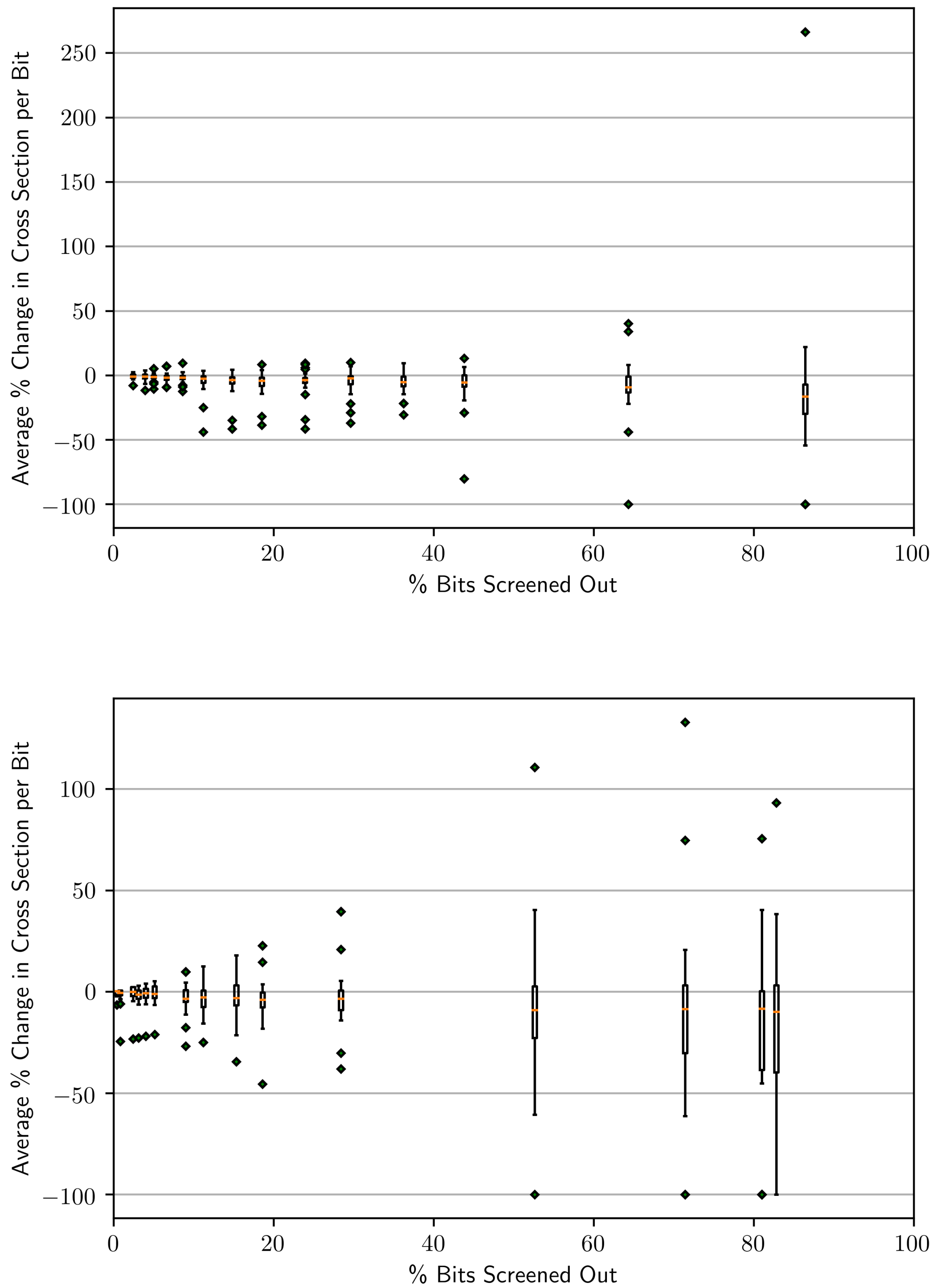

FIGURE 3.9: A plot of the average percentage change in σ_{SEU}/bit as a function of the percentage of bits screened out. RD03 results are shown on top and RD04 on bottom. In all cases, cells with Qc values above a certain threshold are kept and all others discarded. This plot shows all data

CHAPTER 4: Discussion

4.1 Electric results

We have developed an electrical test (sections 2.1.1 and 3.1) to determine the cell by cell relative Q_c by measuring V_{DR} characterizable cells. Cells, in general, have different V_{DR}, dependant on whether they hold a logical '1' or '0', but are consistent across multiple trials for the same logic value. The distributions of three different patterns (0x00, 0xAA, and 0xFF) show no major differences between the aggregate behavior of logic 1's and 0's.

This characterization is not limited by technology type and thus can be applied to a broad category of transistor-based memory devices from 90nm SRAM to 15nm to non-silicon based SRAM as the principles governing these devices are the same.

4.1.1 Virtual Spatial Mapping

Several interesting patterns were picked out of the virtual spatial maps. However, without actual knowledge of the cell's layout on the dye, very little can be said with confidence.

Fig. 4.1 shows four distinct quadrants. This behavior was also captured in DUT AD01 and AD03 but was not present in AT01 or AT02. The explanation for why quadrants might exist lies with the manufacturer and how they lay cells on a dye. Unfortunately, because these are commercial chips, the physical layout of the cells is an unknown quantity. To speculate, however, from de-lidding two of the devices, the dye appears to be split into 4 discrete sections. Fig. 4.2 shows what one of the DIP MicroChip devices looks like under a microscope. This seems to indicate that the DIP MicroChip devices (and the On Semiconductor devices) have a similar underlying architecture that is not shared by the TSSOP devices produced by Microchip.

AD02 0xaa 0.227 Volts

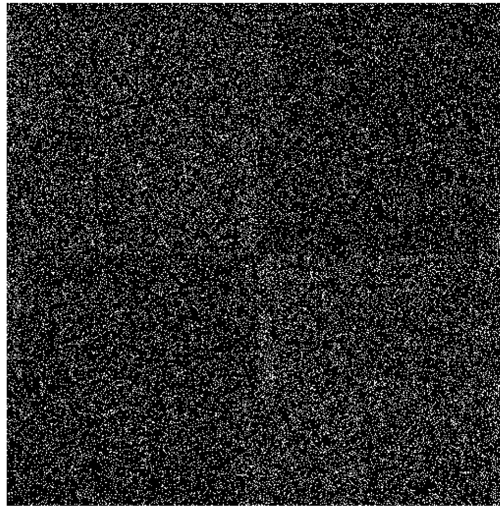

FIGURE 4.1: An image of a virtual spatial map from chip AD02 tested with pattern 0xAA at $V_{hold} = 0.227V$. This shows 4 distinct quadrants with two appearing to have a higher density of cells reporting flips while two appear to have a lower density of flips.

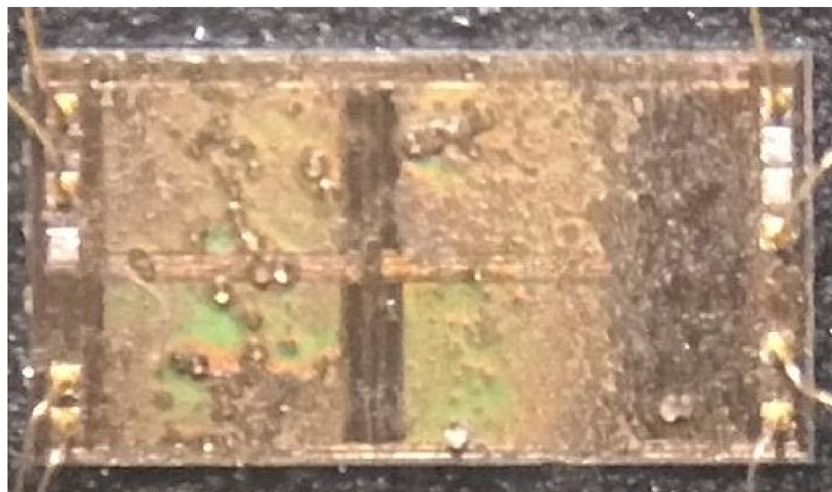

FIGURE 4.2: A picture of one of the de-lidded devices under a microscope. Four rectangular sections are identifiable as potentially being where the cells are located

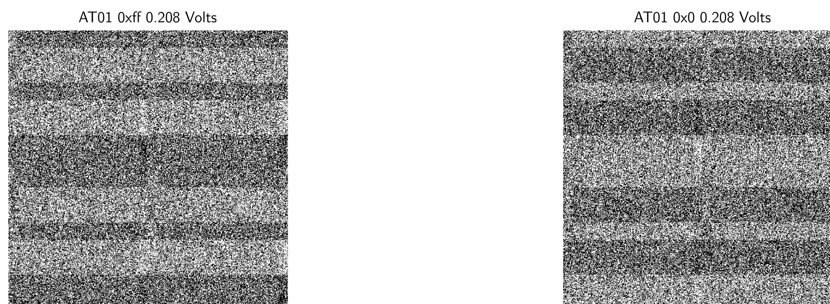

FIGURE 4.3: Two virtual spatial maps for device AT01 both at $V_{Hold} = 0.208V$. On the left is the all ones test pattern and the right is all zeros. Both exhibit striping in the same locations but the relative densities are inverted. Stripes with high densities of bit flips for one pattern have low densities of flips for the opposite pattern

In all components, some amount of pattern specific striping was observed, shown in Fig. 4.3. In these and all cases, the stripes appear inverted when the data pattern is inverted. In 0xFF (all ones), the stripes with the higher density of failures become the stripes with a lower density of failures when 0x00 (all zeros) is checked for instead. This implies a complimentary set of V_{DR} values depending on the data value being held. The striping specifically also implies distinct regions in which the cells behave similarly and, given the mapping presented here, those regions are in logical address order. Being in logical address order presents the possibility of error mitigation without an in-depth look-up table to keep track of each individual cell's Q_c value and rather, a chip can be accessed according to regional behavior.

It is hard to say anything about the underlying physics behind this phenomena with confidence without knowing more about the devices' cell layout, but this phenomena deserves further investigation than is presented in this thesis.

4.2 Radiation Results

We showed that when irradiated by low energy protons, the cells that upset were disproportionately likely to have $Q_c < \overline{Q_c}$ in section 3.2. This shift, while statistically significant in likelihood, is relatively small, with the most drastic shift on

the order of a 1% smaller mean Q_c from $\overline{Q_c}$.

In section 3.3 we showed that applying a virtual screening to remove bits identified with the electrical test as having smaller Q_c values than an arbitrary threshold allowed for the σ_{SEU}/bit to be reduced when compared to a baseline of all electrically characterized cells. As the screening threshold was increased and more cells were removed from the analysis, the cross-section reduced by a greater percentage, although the deviation also increased significantly (Figs. 3.8 and 3.9).

The combination of these results means that a device does not have a single, constant, σ_{SEU}/bit for low energy particles but rather every cell has a unique σ_{SEU}/bit that when aggregated together becomes the historically reported constant σ_{SEU}.

It is important to realize that these results likely do not extend to high energy particles. Mitigating the σ_{SEU}/bit is possible only when the charge deposited by a collision is on the order of the real Q_c of a cell. If the charge deposited is well in excess of the highest Q_c of a device, the probability of upset does not vary from cell to cell.

A cell level variation in Q_c implies strongly that there then exists cell level variation in the threshold LET. At the cell level, an LET curve may more closely resemble a step function with a clear minimum particle LET necessary for upset followed by a near-instantaneous transition to a saturated cross-section. It could then be the aggregate tendency of chips to contain low Q_c skewed distributions, simulated by Wang et al. (2010) and seen in the electrical characterizations presented here, that causes the Wiebull curve seen in standard cross-section data. Then, by appropriately screening out cells with low Q_c, the chip-wide threshold LET could be shifted to the right toward higher values, potentially changing the shape of the LET curve to more sharply approach a saturation of the cross-section.

CHAPTER 5: Conclusion

5.1 Why it All Matters

There are a few reasons the work presented in this thesis is of significant importance. The first of which is almost an underlying assumption: there are cell-to-cell variations in the radiation hardness of SRAM. This is not currently general knowledge in the radiation effects field. Currently, data stored on an SRAM is treated as universally having the same probability of having an upset. Characterizing a chip's cells may allow triaged data storage for space missions. Consider an instrument that takes data in between convenient communication links with the Earth. Instead of writing and holding the data in the SRAM indexing at the 1st address and moving forward, the data could be written from strongest cell to weakest, thereby reducing the probability of an upset causing data loss.

The trade off would mean having to index the memory non-sequentially which, in principle changes nothing within the read/write time of SRAM as a class of Random Access Memory which has identical access times to any bit of data. What it would add, would be some complexity in the code that chooses which cells to access when. This added complexity however is minimal, perhaps as simple as a single function to change the order cells are accessed in, thus adding a likely negligible amount of time to the execution of a program that uses the mitigation strategy proposed here.

Next consider a mission that has some maximum σ_{SEU} allowable that is just out of the range of a commercial chip. Normally, this would force a huge developmental expenditure of time and resources developing a sufficiently radiation hardened alternative. However, with this screening procedure, by sacrificing storage capacity in the weakest subset of bits, an otherwise ineligible commercial part may be able to be modified to fit the mission requirements.

If additional work can be done to link relative Q_c to exact σ_{SEU}, the need to robustly characterize devices via irradiation has the potential to be relaxed. Given

the relative scarcity of facilities capable of doing LET characterization testing, that has the very real possibility of reducing the cost of quality assurance for all forms of space instrumentation.

5.2 Future Work

This project is very exciting because the work presented here is just the beginning. In the near term, the next steps could include replicating the radiation tests presented here but with chips characterized to lower V_{DR} values and for multiple test patterns. This would allow for testing whether a cell with a low Q_c value for a logic 1 is more likely to experience an upset when it has a logic 0 stored than a cell that has a high Q_c for both, something that would line up with Wang et al. (2010)'s definition of V_{DR} being the *maximum* V_{DR} of the V_{DR1} and V_{DR0}.

Additionally, working with custom chips where the mapping from logical address to physical layout on the dye would allow for spatial auto-correlation analysis to see if weak cells are clustered, are the product of edge effects, or any number of other possibilities.

Further out, performing tests at a variety of particle energies would allow for more robust σ_{SEU} measurements. This would also allow the characterization of the effectiveness of a virtual screening as a function of particle energy; the hypothesis here being that as particle energy (more precisely, linear energy transfer, LET) increases, the effectiveness of a virtual screen based on characterized Q_c decreases.

Finally, an immense step forward would be to generalize this sort of characterization and analysis beyond SRAM and into other devices.

5.3 The End

In this thesis, I presented an experimental design to characterize SRAM cell-specific Q_c values via V_{DR} measurements. Then I showed what the data of those characterizations looked like before combining those data with data from radiation

tests performed at the Vanderbilt University Peletron for two SRAM chips. After showing that the cells that upset when irradiated disproportionately favored those characterized as having $Q_c < \overline{Q_c}$ I showed that virtually screening out cells with low Q_c improved the σ_{SEU}/bit for those trials.

APPENDIX A: Board Design

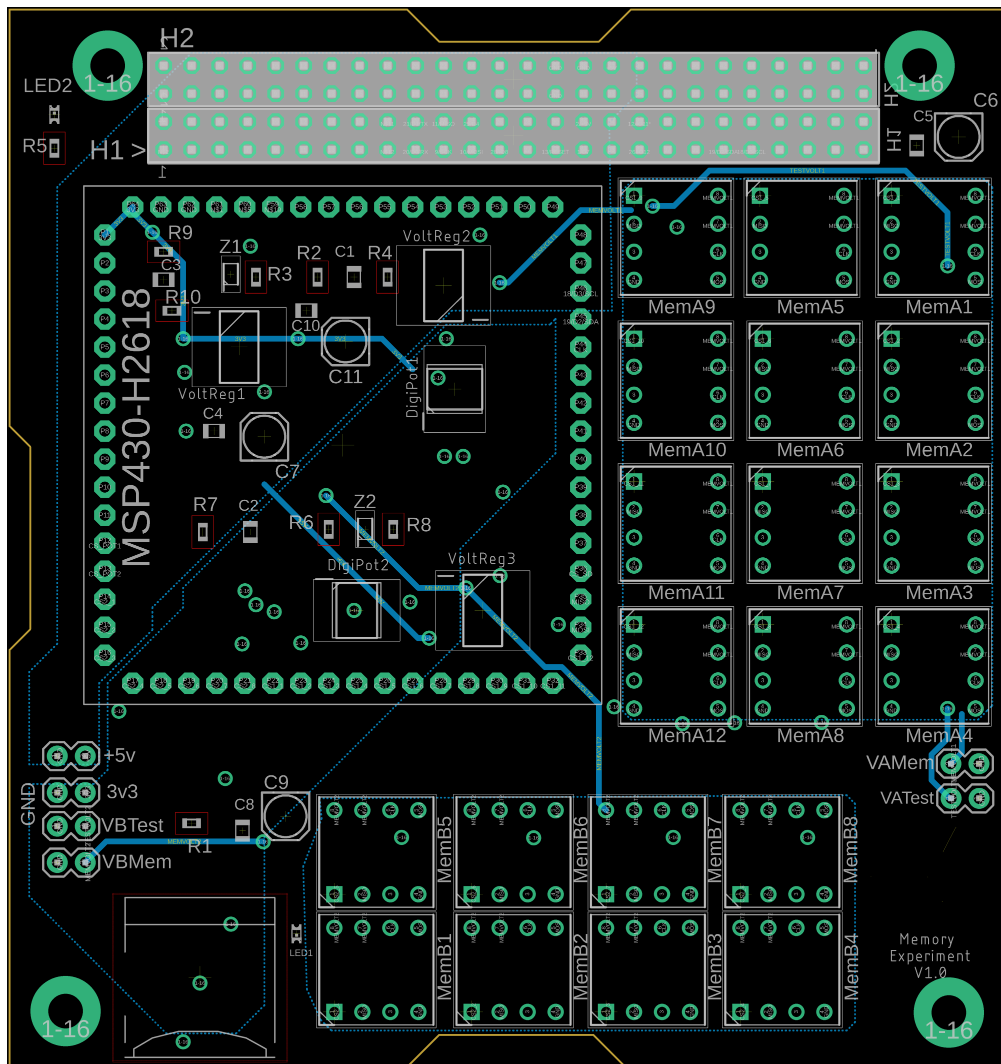

FIGURE A.1: A layout image from the design of the experimental PCB's bottom layer. This layer routes power or DC signals

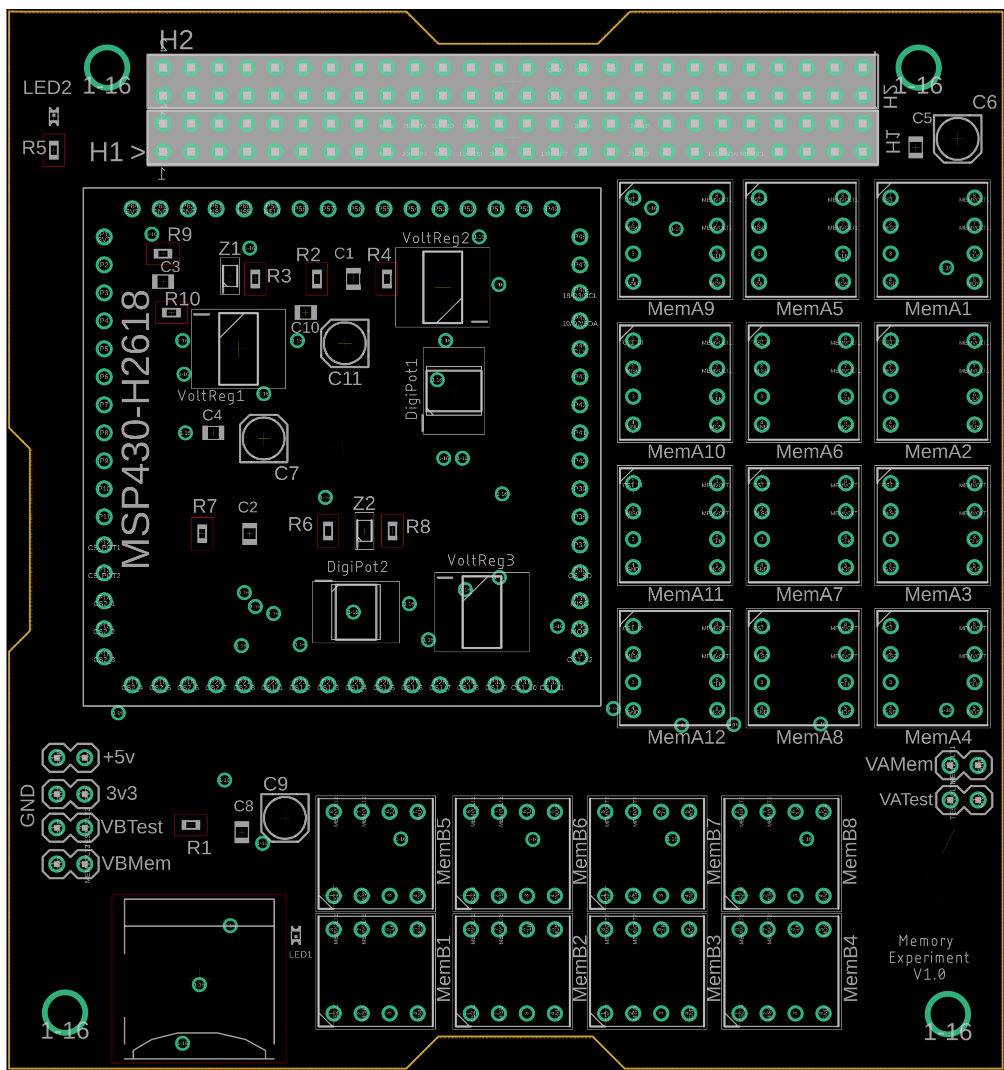

FIGURE A.2: A layout image from the design of the experimental PCB's second layer. This layer is purely a ground plane

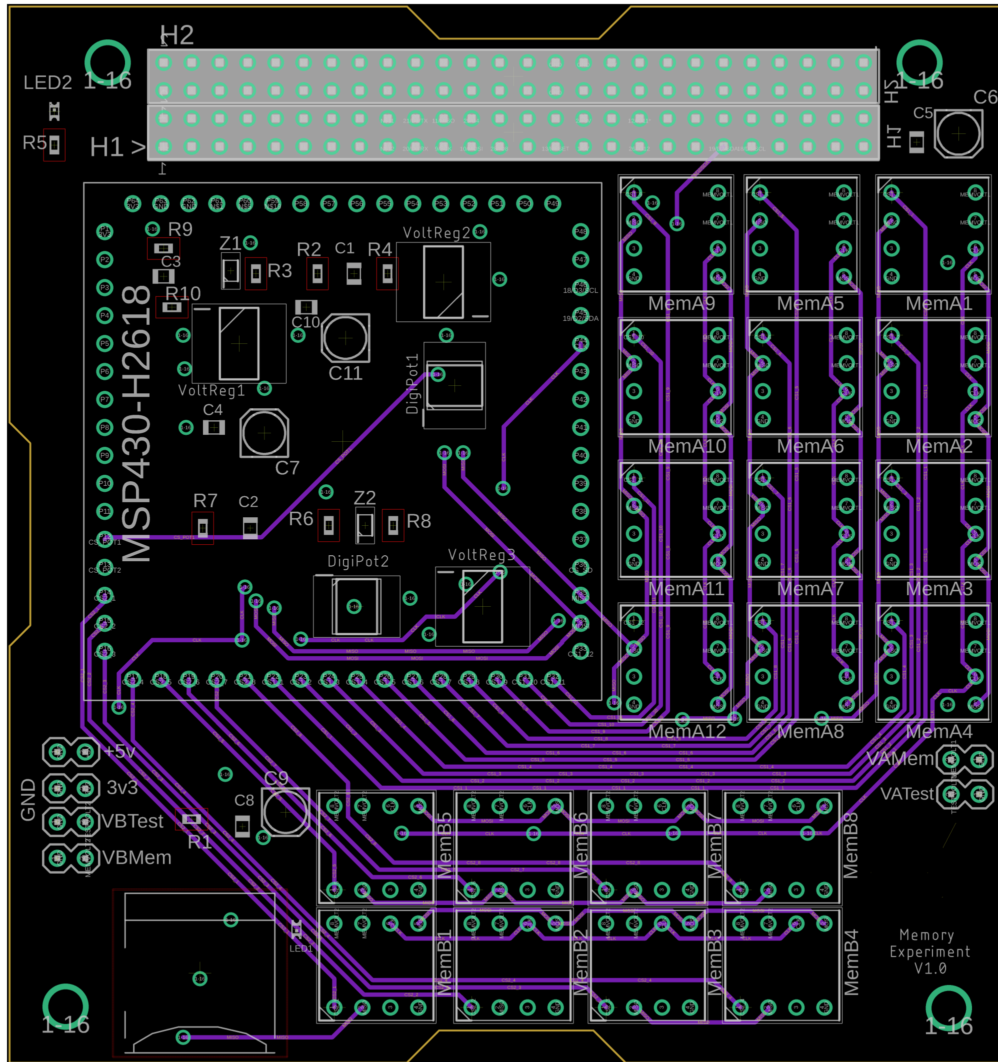

FIGURE A.3: A layout image from the design of the experimental PCB's third layer. This layer handles the majority of the clocked signals

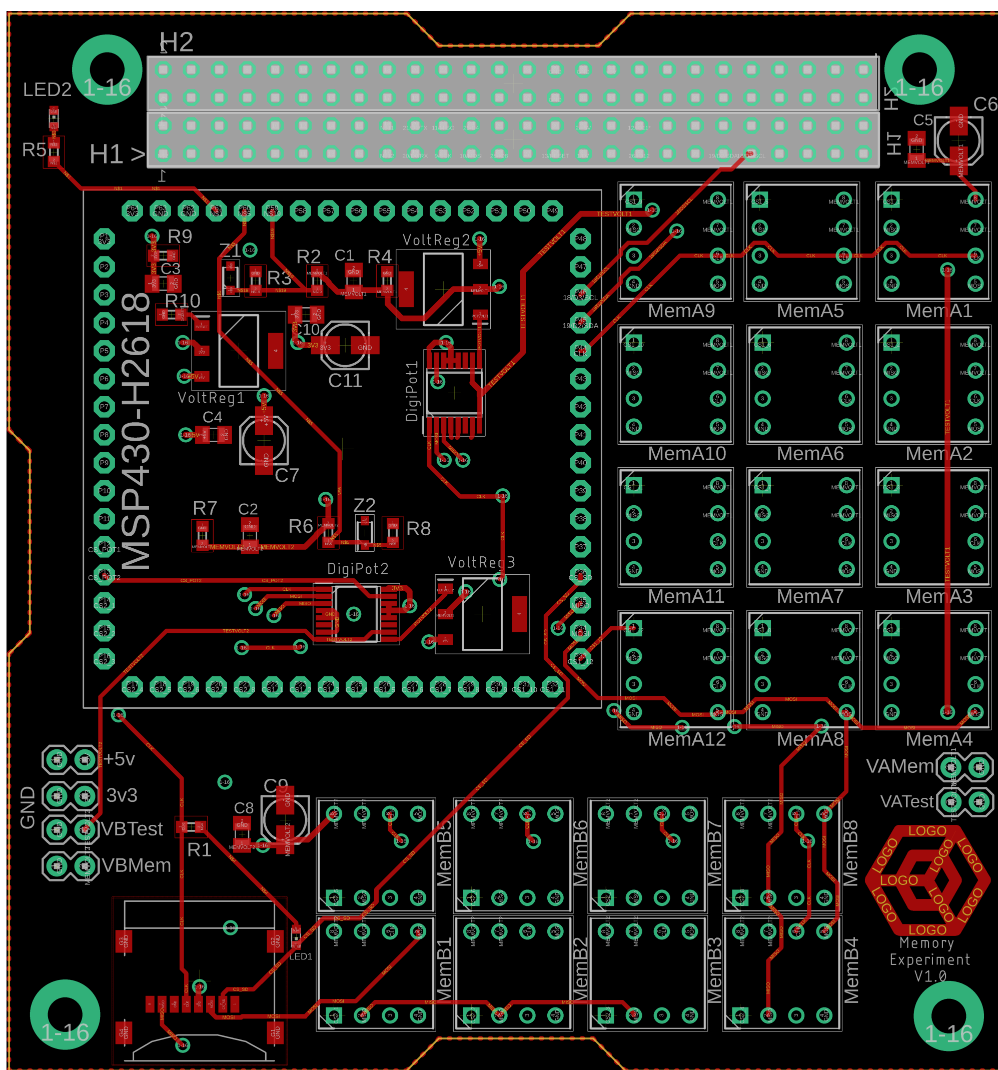

FIGURE A.4: A layout image from the design of the experimental PCB's top layer. This layer handles the final routes to surface mount components

APPENDIX B: Electrical Characterization Figures

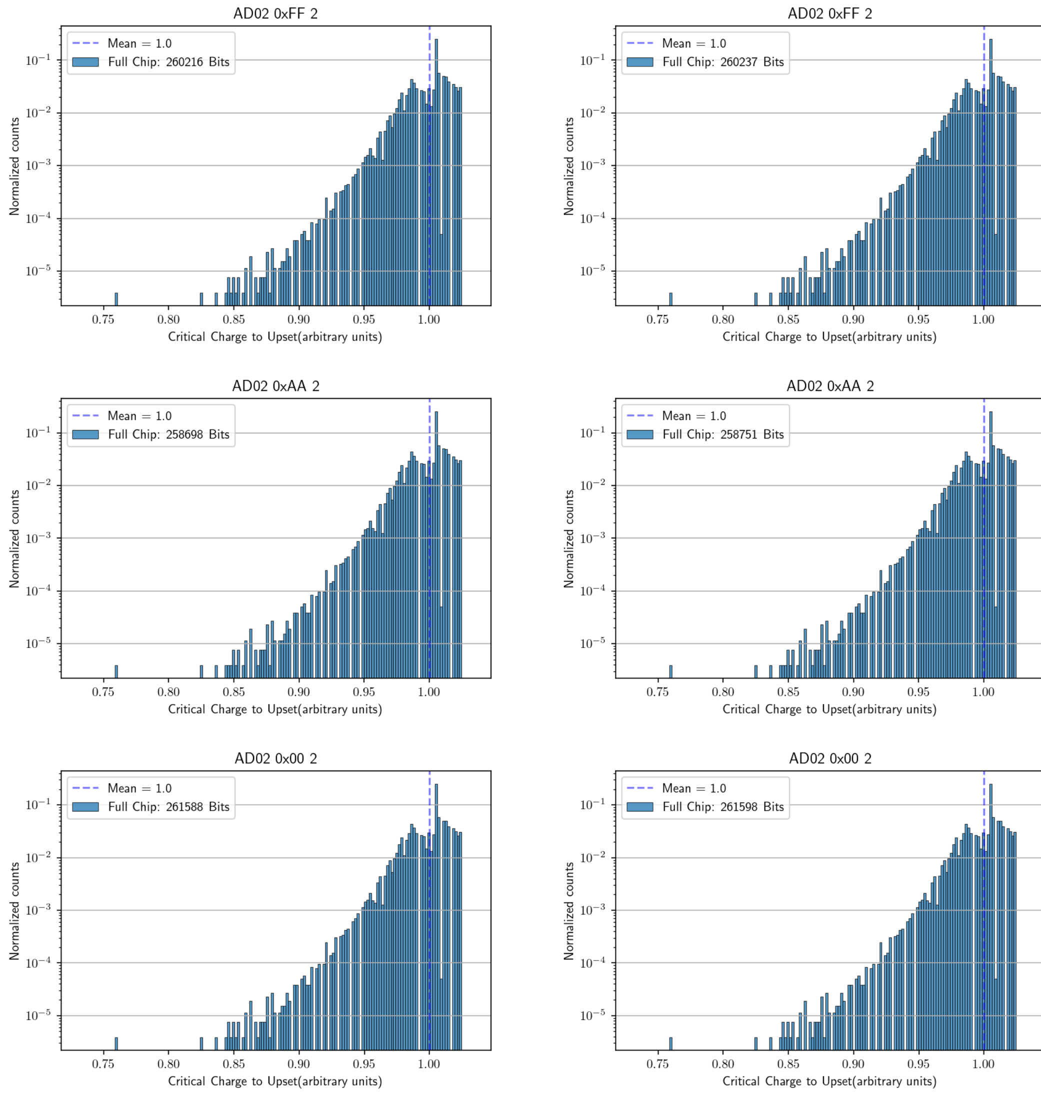

FIGURE B.1: Electrical characterization distributions for AD02 across three patterns each tested twice.

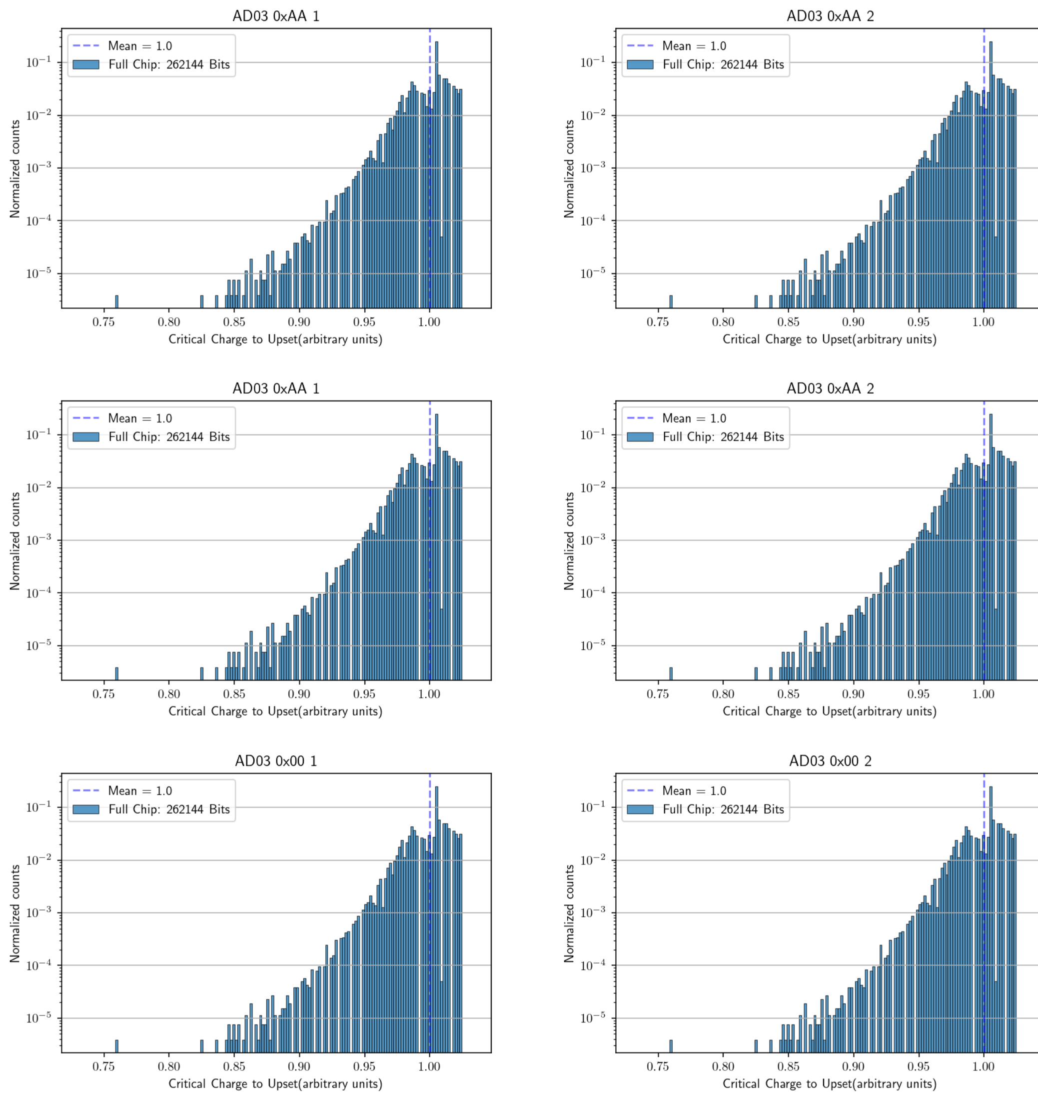

FIGURE B.2: Electrical characterization distributions for AD03 across three patterns each tested twice.

APPENDIX B: Bibliography

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